Amendments to the Claims

Claims 1-37 (Canceled).

38. (Currently Amended): Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

an insulative layer received over the word lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area, the well having a substantially planar base;

a plurality of memory cell storage capacitors received within the one well, the memory cell storage capacitors respectively comprising a storage node container which is received partially within the insulative layer through the well base over the word lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

39. (Original): The memory circuitry of claim 38 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

40. (Original): The memory circuitry of claim 38 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

41. (Original): The memory circuitry of claim 38 comprising buried digit lines, the well base having a lowest portion which is received at least 1000 Angstroms above outermost tops of the digit lines.

42. (Previously Presented): Dynamic random access memory circuitry comprising:

a semiconductor substrate;

word lines received over the semiconductor substrate;

~~bit~~ digit lines received over the word lines;

an insulative layer received over the word lines, the digit lines and the substrate, the insulative layer having at least one well formed therein, the well comprising a base received over the word lines and the digit lines, the well peripherally defining an outline of a memory array area, area peripheral to the well comprising memory peripheral circuitry area;

a plurality of memory cell storage capacitors received within the one well over the word lines and the digit lines; and

peripheral circuitry within the peripheral circuitry area operatively configured to write to and read from the memory array.

43. (Original): The memory circuitry of claim 42 wherein the insulative layer has a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally proximate the substantially planar outermost surface of the insulative layer.

44. (Original): The memory circuitry of claim 42 wherein the insulative layer is formed to have a substantially planar outermost surface, and the capacitors have capacitor storage node electrodes having topmost surfaces received elevationally above the substantially planar outermost surface of the insulative layer by less than 50 Angstroms.

Claims 45-47 (Canceled).

48. (New): The memory circuitry of claim 38 wherein the insulative layer comprises SiO_2, and further comprising an Si_3N_4 comprising layer received on the well base.

49. (New): The memory circuitry of claim 48 wherein the Si_3N_4 comprising layer has a thickness of from about 40 Angstroms to about 125 Angstroms.

50. (New): The memory circuitry of claim 48 wherein the Si_3N_4 comprising layer has a thickness of from about 50 Angstroms to about 70 Angstroms.

51. (New): The memory circuitry of claim 42 wherein the insulative layer comprises SiO_2, and further comprising an Si_3N_4 comprising layer received on the well base.

52. (New): The memory circuitry of claim 51 wherein the Si_3N_4 comprising layer has a thickness of from about 40 Angstroms to about 125 Angstroms.

53. (New): The memory circuitry of claim 51 wherein the Si_3N_4 comprising layer has a thickness of from about 50 Angstroms to about 70 Angstroms.

54. (New): The memory circuitry of claim 38 wherein one of the storage node electrodes is spaced laterally inward of the outline peripherally defined by the well thereby forming a space between said one electrode and said outline.

55. (New): The memory circuitry of claim 42 wherein the one of the storage node electrode is spaced laterally inward of the outline peripherally defined by the well thereby forming a space between said one electrode and said outline.